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APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that We, Yongsoo CHO and Seung-Ho HAHN, citizens of Korea, residing at #103-1103 Gangbyeon APT., Mannyeon-dong, Seo-gu, Daejeon 302-741 KOREA and #126-1004 Byoksan APT., Yeonwonmaeul, Guseong-eup, Yongin-si, Gyeonggi-do, 449-938 KOREA respectively, have invented a new and useful **METHOD OF FABRICATING A MOSFET**, of which the following is a specification.

METHODS OF FABRICATING A MOSFET

TECHNICAL FIELD

[0001] The present disclosure pertains to methods of fabricating a semiconductor device and, more particularly, to methods of fabricating a metal-oxide-semiconductor field effect transistor (hereinafter referred to as "MOSFET") that is able to ensure an effective channel length.

BACKGROUND

[0002] Line width in semiconductor devices has been continuously reduced due to high integration of semiconductor devices. As the line width in a gate electrode shrinks, the length of the channel decreases. In addition, the threshold voltage starts to decrease appreciably with the channel length. This phenomenon is typically called the "short channel effect." Accordingly, various technologies to reduce such short channel effect have been proposed.

[0003] Preferably, the short channel effect is obviated for high integration of a semiconductor device. An example of a method for obviating the short channel effect is to form lightly doped drain (LDD) regions.

[0004] Figs. 1a through 1d are cross-sectional views illustrating a process of fabricating a MOSFET with LDD regions. Referring to FIG. 1a, a gate oxide layer 2a and a polysilicon layer 2b as a conducting layer for a gate, are formed on a semiconductor substrate 1. The polysilicon layer 2b and gate oxide layer 2a are etched to form a polysilicon gate electrode 3. Then, as shown in FIG. 1b, a low-concentration

ion implantation and a thermal treatment process are used to form LDD regions 6 on the surface of the substrate at both sides of the polysilicon gate electrode 3.

[0005] Next, referring to FIG. 1c, the whole area of the semiconductor substrate 1 including the polysilicon gate electrode 3 is covered with an insulating layer, and the insulating layer is blanket-etched to form a gate spacer 5 on both lateral walls of the polysilicon gate electrode 3. Then, as shown in FIG. 1d, a dopant is implanted into the substrate part at both sides of the polysilicon gate electrode 3 including the spacer 5 by means of high-concentration ion implantation. After the ion implantation, a thermal treatment process is conducted to form source and drain regions 8 having LDD regions 6.

[0006] However, in the above-described method of fabricating a MOSFET, it is difficult to ensure an effective channel length because the LDD regions and source and drain regions are formed by ion implantation and thermal treatment.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIGS. 1a-1d are cross-sectional views illustrating one process of fabricating a MOSFET.

[0008] FIGS. 2a-2e are cross-sectional views illustrating another process of fabricating a MOSFET.

DETAILED DESCRIPTION

[0009] The present disclosure is directed to a method of fabricating a MOSFET that is able to ensure an effective channel length. The disclosed method includes (1) forming a polysilicon gate electrode on a semiconductor substrate; (2) forming a first doping layer on the whole area of the semiconductor substrate including the polysilicon gate electrode; (3) implanting some dopant into the first doping layer by means of a high-tilt angle pocket ion implantation; (4) forming LDD regions on the surface of the substrate at both sides of the polysilicon gate electrode by diffusing the dopant of the first doping layer into the semiconductor substrate at the same time as forming an insulating layer on the first doping layer; (5) forming a spacer by etching the insulating layer and the first doping layer; (6) forming a second doping layer on the semiconductor substrate and the polysilicon gate electrode with the spacer; and (7) forming source and drain regions on the surface of the semiconductor substrate at both sides of the polysilicon gate electrode with the spacer by conducting a thermal treatment process so that the dopant of the second doping layer can be diffused into the semiconductor substrate.

[0010] The first doping layer may be made of silicated glass with a dopant. For example, borosilicate glass (BSG) or phosphosilicate glass (PSG) may be used for the first doping layer. As a result, the LDD regions can be formed, without further thermal treatment, by diffusing the dopant of the first doping layer into the substrate when the subsequent insulating layer is formed. The second doping layer is an oxide layer and may be formed by means of a plasma enhanced chemical vapor deposition (PECVD) process. As a result, the source and drain regions can be formed by

diffusing the dopant of the second doping layer into the substrate by means of a subsequent thermal treatment.

[0011] Referring to the example illustrated in FIG. 2a, a gate oxide layer 22a and a polysilicon layer 22b as a conducting layer for a gate, are formed on a semiconductor substrate 21. The semiconductor substrate may be, for example, Si, GaAs or silicon-on-insulator. Then, the polysilicon layer 22b and the gate oxide layer 22a are etched to form a polysilicon gate electrode 23.

[0012] Referring to the example illustrated in FIG. 2b, a first doping layer 24 is coated on top of the whole area of the semiconductor substrate 21, including the polysilicon gate electrode 23. The first doping layer 24 may be made of, for example, BSG or PSG.

[0013] Referring to the example illustrated in FIG. 2c, a dopant is implanted into the first doping layer by means of a high-tilt angle pocket ion implantation. The pocket ion implantation may be performed with an angle between 5° and 45°. The dopant may be, for example, B, BF_2, P, As or N. Then, an insulating layer 25 is formed on the first doping layer 24. For example, a low pressure chemical vapor deposition (LPCVD) process may be used. The dopant which is doped into the first doping layer 24 is diffused into the semiconductor substrate 21 to form LDD regions 26 on the surface of the substrate at both sides of the polysilicon gate electrode 23.

[0014] Referring to the example illustrated in FIG. 2d, the insulating layer 25 and the first doping layer 24 are etched to form a spacer 25a. As an example, the thickness of the spacer may be between 50 and 500 Å.

[0015] Next, referring to the example illustrated in FIG. 2e, the semiconductor substrate 21 and the polysilicon gate electrode 23 including the spacer 25a are covered with a second doping layer 27. The second doping layer 27 is an oxide layer that may be formed, for example, by means of a PECVD process. As an example, the thickness of the second doping layer may be between 100 and 1000 Å. Subsequently, a rapid thermal process is conducted to form source and drain regions 28 with shallow depths on the surface of the semiconductor substrate 21 at both sides of the polysilicon gate electrode 23 having the spacer 25a. As an example, the thermal treatment may be performed at a temperature between 950 and 1150 ℃ for 3 to 20 seconds.

[0016] In the method disclosed herein, LDD regions are formed by diffusing the dopant of the first doping layer into the semiconductor substrate. In addition, source and drain regions are formed by diffusing the dopant of the second doping layer. As a result, effective channel length is more ensured compared to methods which form LDD regions, source regions, and drain regions by means of an ion implantation and a thermal treatment.

[0017] Thus, the present method is useful, for example, for fabricating a MOSFET having a gate electrode of length of less than 0.1 ㎛, and the present method can obviate a short channel effect and a reverse short channel effect. In addition, the present method does not require a thermal treatment process to form LDD regions or an ion implantation process to form source and drain regions because these regions are formed by diffusion of dopant. As a result, the present method simplifies the wafer fabrication processes.

[0018] The foregoing embodiments are merely exemplary and are not to be construed as limiting. The present teachings can be readily applied to other types of apparatuses. The description herein is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. This patent covers all methods fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.